Daniel Andrasz

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EDUCATION

University of Illinois at Urbana-Champaign Expected May 2027
Bachelor of Science in Materials Science & Engineering 3.59 GPA
Minor in Semiconductor Engineering

- **Relevant Coursework:** Compound Semiconductors & Devices, IC Device Theory & Fabrication, Physics & Modeling of Semiconductor Devices, Plasma Engineering, MEMS-NEMS Theory & Fabrication

WORK EXPERIENCE

AMD (Advanced Micro Devices) Austin, TX
Foundry Technology & Product Optimization Co-Op June 2026 – Present

- Refactored legacy Python layout analysis pipeline, accelerating execution time by $\geq$50% and integrating GUI to streamline execution workflows for cross-functional teams
- Formulated cross-layer chain detection algorithm with machine learning model to pinpoint physical die locations and specific tiles with structural anomalies
- Utilized semiconductor device physics to correlate layout density variations with silicon failure modes, collaborating closely with TSMC to communicate physical defect modes and drive product yield improvements

University of Illinois Urbana-Champaign Champaign, Illinois
Research Assistant, Photonic Systems Laboratory August 2025 – Present

- Led undergraduate thesis on photoelectrochemical etching of intrinsic Si, independently designing full process flow including plasma surface preparation, HF wet etching, e-beam metal deposition, thermocompression wafer bonding, and tube furnace annealing
- Executed mask aligner, maskless photolithography, wet/dry etching, and thin-film deposition in support of ongoing lab research

Teaching Assistant, ECE 385 & ECE 220 August 2024 – May 2026

- Mentored students in SystemVerilog RTL design, FPGA synthesis via Xilinx Vivado, and board-level hardware bringup
- Facilitated hands-on troubleshooting of clock domain crossing (CDC) issues, timing closure violations, memory controllers, and low-level C/Assembly memory-mapped I/O architectures

Texas A&M University College Station, Texas
Research Assistant, Thermal Engineering Group May 2025 – August 2025

- Designed CAD layouts for custom heater geometries and collaborated directly with an external photomask manufacturer to execute tapeout and deliver cleanroom-ready photomasks optimized for thermal test vehicle fabrication
- Tested and validated thermal test vehicles across temperature sweeps of 300-400K, characterizing thermal resistance and electrical behavior under thermal stress via 4-point-probe measurements

PROJECTS

CMOS Integrated Circuit Wafer
Cleanroom, Photolithography, Diffusion, Metrology

- Fabricated integrated circuits from scratch in a Class 100/1000 cleanroom using a 5-mask process sequence (RCA clean, boron/phosphorus thermal diffusion, gate oxidation, aluminum metal evaporation, and lift-off)
- Conducted automated wafer-level I-V/C-V testing using Keithley 4200-SCS parameter analyzers and probe stations, extracted V_{th}, mobility, sheet resistance, and breakdown voltage across 50+ test structures
- Correlated physical failure modes (pinholes, oxide breakdown, diffusion shorts) to fabrication anomalies, maintaining a $\sim$75% functional device yield across variable channel length devices

NES Hardware Emulator on FPGA
SystemVerilog, Xilinx Vivado, Vitis, FPGA

- Designed and validated a cycle-accurate NES digital architecture in SystemVerilog, implementing custom RTL for the Picture Processing Unit (PPU), APU audio synthesis, and USB gamepad logic
- Resolved complex timing violations and bus contention issues across memory-mapped I/O interfaces, verified NTSC composite video generation and scanline timing using digital logic analyzers

AI-Powered Wafer Map Defect Classification & Visualization Framework
Python, PyTorch, Computer Vision, Grad-CAM, Streamlit

- Built an end-to-end PyTorch pipeline using ResNet-18 CNN to classify 8 spatial wafer defect patterns from the WM-811K dataset
- Integrated Grad-CAM to generate spatial heatmaps isolating defect root causes for fab engineers, mitigating "black-box" AI risks

SKILLS

- **Semiconductor Fabrication:** Photolithography (Mask/Maskless), RIE/Plasma Etching, HF/BOE Wet Etching, E-beam Deposition, Thermal Oxidation, Thin-Film Deposition, Thermocompression Bonding, Tube Furnace Annealing, Spin Coating, Lift-off, Diffusion
- **Characterization & Metrology:** I-V/C-V Profiling, Parameter Extraction, 4-Point Probe, Probe Station, Interface Defect Analysis, Yield Analysis, DFM
- **Programming & Tools:** JMP, Snowflake, Python (NumPy, SciPy, Pandas, Matplotlib), Sentaurus, SystemVerilog, C/C++, LaTeX, Vivado, ModelSim, SolidWorks